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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/555,301	05/26/2000	MARKUS FEUSER	PHD99-097	3809

7590 06/03/2004

Philips Electronics North American Corp.
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Tarry town, NY 15091

EXAMINER	
DADA, BEEMNET W	

ART UNIT	PAPER NUMBER
2135	7

DATE MAILED: 06/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/555,301	FEUSER, MARKUS	
	Examiner	Art Unit	
	Beemnet W Dada	2135	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 April 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reiner (US Patent No. 5,995,629).

3. As per claims 1 and 3, Reiner teaches a method of operating a data processing device, which includes an integrated circuit, which carries out in dependence on clock signal, arithmetic operations for cryptographic operations, data input and data output as well as data transfer from and to registers of the integrated circuit [column 2, lines 12-27]. Furthermore, Reiner teaches the integrated circuit controlled in such a manner that the execution of actual encoding operations on one hand and data transfer from the encoding device into output register on the other hand are execute in parallel (i.e., actual arithmetic operations executed during a first time period and data transmission performed within a second time period, wherein second time period lies within the first time period) [column 2, lines 24-29 and column 4, lines 7-29], and after the first time period ends, the integrated circuit continues to generate output data, that are no longer written into the output register, while the output register performs data shifting (i.e., the

integrated circuit or registers of the integrated circuit generate dummy data on one hand and the output shift register performs data shifting on the other hand, in parallel) [column 4, lines 13-24].

Reiner does not explicitly teach executing actual arithmetic operations on one hand and dummy data transfer from one register to another on the other hand executed in parallel in time. It would have been obvious to one having ordinary skill in the art at the time the invention was made to execute actual arithmetic operations on one hand and dummy data transfer from one register to another on the other hand executed in parallel in time. It would have been obvious because Reiner teaches execution of actual encoding operations on one hand and data transfer from the encoding device into output register on the other hand execute in parallel [column 2, lines 24-29 and column 4, lines 7-29], and generating dummy data on one hand performs data shifting on the other hand, in parallel [column 4, lines 13-24]. Based on this teaching it would have been obvious to one having ordinary skill in the art at the time the invention was made to execute actual arithmetic operations on one hand and dummy data transfer from one register to another on the other hand executed in parallel in time, in order to disguise power consumption of a device.

4. As per claim 2, Reiner teaches the method / device as applied above. Furthermore, Reiner teaches the method characterized in that during actual data transfer from one register to another or between registers of the integrated circuit, a processor of the integrated circuit generates dummy data, no data being written into registers of the integrated circuit [column 4, lines 7-29].

5. As per claim 3, Reiner teaches the method as applied above. Furthermore, Reiner teaches an operand register of the processor and/or a register for data input/output [figure1, units AK, SR, RK and AR].

Response to Arguments

6. Applicant's arguments filed April 5, 2004 have been fully considered but they are not persuasive.

7. With respect to claims 1, 3 and 4, the applicant argues that claims 1 and 3 are amended to particularly recite executing actual arithmetic operations on the one hand and dummy data input/output operations or dummy data transfer on the other hand from one register to another on the other hand in parallel. Further, the applicant argues that Reiner generally describes an encoding device that performs dummy encoding operations in an encoding unit during such time that data shifting operations are performed in an output register. The examiner respectfully disagrees.

Reiner teaches an integrated circuit controlled in such a manner that the execution of actual encoding operations on one hand and data transfer from the encoding device into output register on the other hand are execute in parallel (i.e., actual arithmetic operations executed during a first time period and data transmission performed within a second time period, wherein second time period lies within the first time period) [column 2, lines 24-29 and column 4, lines 7-29], and after the first time period ends, the integrated circuit continues to generate output data, that are no longer written into the output register, while the output register performs data shifting disguising power consumption during encoding operations (i.e., the integrated circuit or registers

of the integrated circuit generate dummy data on one hand and the output shift register performs data shifting on the other hand, in parallel) [column 4, lines 13-24]. Based on this teachings it would have been obvious to one of ordinary skill in the art to implement execution of actual arithmetic operations on one hand and dummy data input/output on the other hand to disguise power consumption during actual arithmetic operations.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Beemnet W Dada whose telephone number is (703) 305-8895. The examiner can normally be reached on Monday - Friday (8:30 am - 6:00 pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Y Vu can be reached on (703) 305-4393. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Beemnet Dada

May 26, 2004

KIM VU
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100